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Throughput Testbench Setup Development For Memory Expansion Of Gensets

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Abstract: In power generation industry, there is a huge demand regarding variation of Customer requirements/ feedback which needs of developing and modifying the software scripts. Adding Genset functions in software script causes Genset memory capacity on brink and it will be insufficient to add more smart functions to the Genset. Therefore in order to suffice the latest market needs, memory expansion is vital for the legitimate performance of the Genset. Further these causes heavy load on the framework of a Genset function and thus increases the execution time which may decline the performance of the Genset. This paper describes about the implementation of external memory and the intense approach reducing the execution time with the help of Throughput test setup. Hardware-in-the-loop (HIL) testing approach in the design of power electronics i.e. throughput setup is used which gives the real time simulation environment. Moreover, the setup interprets the particular task in a framework having overload task affecting the performance.In addition, generate the Throughput log of Memory expanded Genset boards in the database system for comparison and use it to correlate with existing Genset boards to review the ‘unskipped frame’ for achieving the goal of zero failure. Thus, obtaining the lower Throughput value eventually reduces the execution time for consistent behavior of Gensets. Finally, the canny way of Throughput testing for Memory Expansion of Genset is summarized here.

Keywords: Hardware-In-Loop (HIL), Memory Expansion, Throughput of Gensets, Fault Code Analysis.

I. INTRODUCTION

In the present generation, digital world is an important aspect for progress of technology and it has become inevitable for every person to rely on the digital devices. These devices require a memory to save the data and relying more on digital zone has caused insufficient memory for the best possible working of the device having advance features.Further, the need arises for memory expansion of the devices without affecting its performance by lowering the propagation delay between input and output of the system. Similarly, in this Case study Genset board has a memory of 512Kb and due to huge requirements from the customer, it is impossible to add these requirements i.e. smart features in the current Memory capacity of Genset. Thus, there is a requirement of Memory Expansion on Genset board.
Hardware-In-Loop (HIL) testing is a technique which replaces the Plant model of physical system with the software model that exactly describes the complete behavior of the physical plant. A power electronics HIL environment provides a prototyping platform for the testing of power electronics hardware, software, and firmware. The HIL models are interfaced with an Electronic Control Module through the associated hardware and software to simulate actuators and sensors. Figure-1 shows a generalized block diagram of the throughput testbench. The main purpose with the HIL Simulation is to test the hardware device on a simulator before we implement it on the real process.

Throughput refers to how much data can be transferred from one location to another in a given amount of time. It also refers to the amount of load it can handle in a particular time frame. For every application there are lots of functions performing simultaneously. To ensure its efficiency, load and performance testing is the solution by simulating the load condition on the HIL system. Currently used Genset boards suffice the need of power generation with a throughput value of approximately 60% which is required for proper functioning of the Gensets. The boards having external memory will provide high propagation delay, finally affecting the throughput. So to achieve the desired Throughput range of 50% - 60% of Memory expanded boards, there is a necessity to determine the unbalance frame of a function which is accomplished by the throughput testbench setup. The HIL test bench consists of integration of hardware and Software setup. Hardware setup consists of the Genset boards which has external memory embedded on it. Further, the throughput values which are derived from the testbench are compared with the throughput values of the currently used Genset boards. Acquiring the throughput values shows the appropriate functioning of hardware. The desired range of throughput values of the boards having external memory should be in the range of 50% - 60% and moreover if these values crosses the desired range, the modification in the test scripts / software is to be done for achieving desired value. The memory efficient throughput values are determined by the monitoring tool used for Genset testing.

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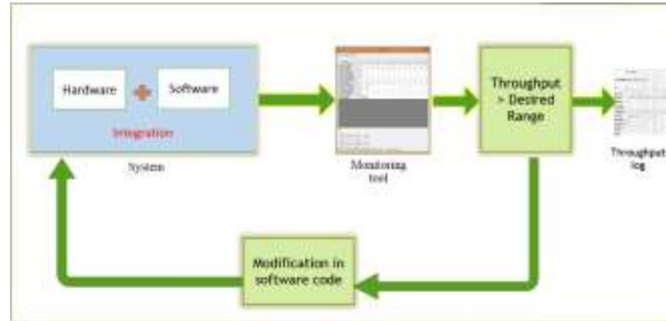

Figure-1 Generalized Block diagram of HIL Testbench

II. MEMORY EXPANSION MODULE

The present Genset boards have a sufficient memory which suffice the need of power generation but it's insufficient to embed the smart features like paralleling, power transfer control. So to provide advance feature of the Gensets and to withstand in the market with the highest priority, Memory expansion is important. Addition of external memory is vital as internal memory expansion is incompatible with the processor used on the Genset boards.

Moreover, Processor-compatible memories does not require significant technology enhancements for digital logic design with respect to standard processes. Integration of these memories with practical units is forthright on a single chip. Dedicated-process memories require process changes and technology enhancements to be integrated with the logic. Figure-2 shows the Block diagram of Memory Expansion.

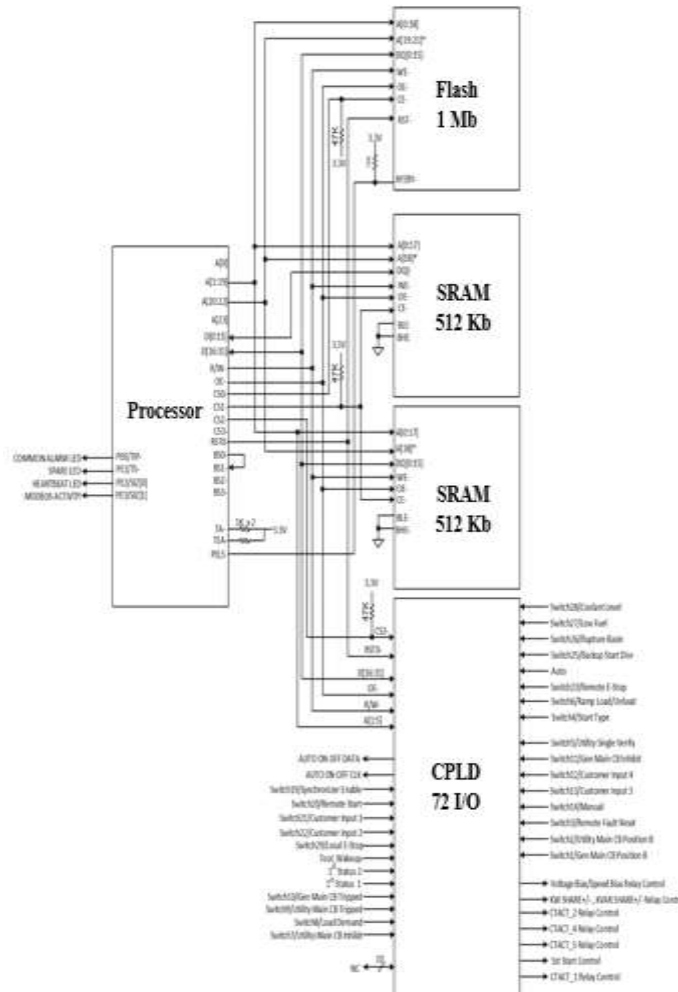

Figure-2 Block diagram of Memory Expansion

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When the processor is turned on, the system is booted from the external Flash to Gensets external SRAM. As soon as a command is received to the processor, the required function is loaded into the SRAM from the flash i.e. Memory management for calculation depends on the Chip select line w.r.t. the priority of the tasks and the time required for execution. External Flash used in the hardware setup is a parallel NOR flash which has a faster Read operation rather than NAND flash having high Write and Erase speed. The execution time of the command is the propagation delay i.e. the time required by the processor for fetching the data from the External SRAM.

III. PLATFORM FOR THROUGHPUT SETUP

Platform for Throughput Setup is explained in two sections viz. Hardware setup and Scripting technique.

A. Hardware Setup

Figure-3 shows the Hardware-In-Loop (HIL) testbench setup for the Throughput testing. HIL testing with the ECM is done for simulating hardware device before implementing it on-field.
The hardware implementation for testing requires a Simulator board as a Master less load demand (MLD), 'N' number of production Genset boards (Load) for ensuring the efficiency. Along with it, Wedge Simulator is used for simulating the board depending on the fault code generation, Engine Control Module (ECM) which reads or interprets the data using lookup tables. Also monitoring device is required for Human –Machine Interface to read the throughput value and monitor the fault code generation. All the devices are interconnected with a wiring harness made for particular device.

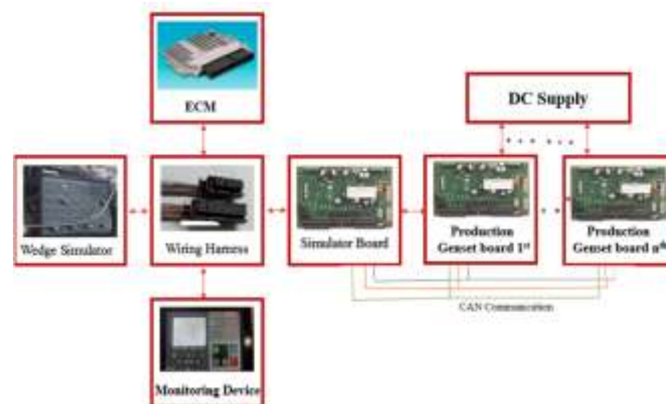

Figure-3 Hardware-In-Loop test bench setup for throughput testing.

Further, MLD board and the Loads communicate with each other by CAN communication. Various configurable function are added with the help of connecting Auxiliary devices. RS-232 protocol, Modbus protocol is used to check the utility of a Modbus register in a Genset.

B. Scripting technique

Consider a Semaphore i.e. a single frame from a cycle of time frame.Figure-4 shows the technical flow process for interpreting data of Semaphore.The first step is to start the execution process of a Semaphore. Initially, a semaphore count is set to zero from a cycle of 500 frames along with an array of certain frequencies. Further, the occurrence of fault code is determined by interpreting the unbalanced case of a frame by performing the following operation.

$$500/X[i] = N \text{ cases}$$

$$\text{Frame Number } \% \text{ N cases} = \text{Case Number (M) of Unbalanced frame}$$

According to the calculated unbalanced case number (M) the corresponding function of the case is modified and updated in the subsequent semaphore. These process continues for particular frequency of each Semaphore. In the next step if the Minor Semaphore count is less than 500, its value is incremented else it will check for consecutive Semaphore.
The estimation of number of cases depends on the Scheduling of the cases in a frame as shown in Figure-5. A particular Semaphore (frame) in a cycle of Framework is of 2ms whereas, each partition of a Semaphore is termed as Minor Semaphore.
A partition of frame denotes numbers of cases (functions) to be executed in a Semaphore which depends on the selection of frequency for execution of function in a cycle.

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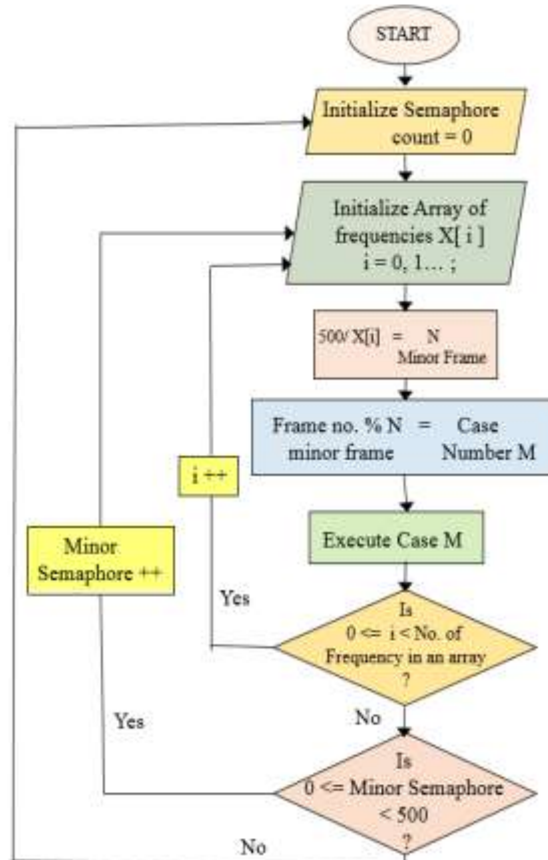

Figure-4 Technical flow for interpreting data of Semaphore

Let say, a function requires a frequency of 250Hz, this denotes a particular frame will execute two cases in a single frame i.e. two functions can be executed in that frame. Similarly, a function having frequency 100Hz will execute five cases in a frame depending on the priority of the function required.

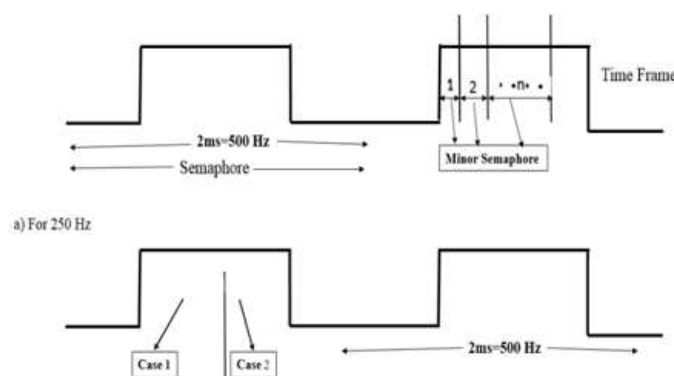

Figure-5 Scheduler Task

IV. SIMULATION AND RESULT

To monitor the throughput test values, skipped frame value and blown frame value are counted with the help of monitoring tool. The flowchart of figure-5 shows the Technical flow process of monitoring tool of time frame.Initially, blown frame and skipped frame values are reset. In the next step interrupt counter starts and the frame of that interrupt is recorded. After execution of interrupt process, execution of time frame is calculated. Moreover, if the frame execution time exceeds the default provided frame time value i.e. it starts the counter for Blown frame and skipped frames after exceeding the frame time value of 2ms and 4ms respectively else it executes the next frame. This process continues till the frame count in a cycle is completed.

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The occurrence of the unstable case in a time frame results in excess load of operation which ultimately increases the throughput value. Moreover it may also generate a fault code while initializing the simulation process.The commonly arise fault code are Excitation Fault, Genset CT ratio low, Short Circuit, CAN Data Link Failure, Update Cal required.

Mon-itor - []

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Array Element -->	0	1	2	3	4
unBlownFrameCount[]##Metrics	0	0	0	0	0
unBlownFrameList[]##Metrics	398	398	388	338	335
unBlownFrameReset##Metrics	0				
unFramePercentAverage##Metrics	56				
unFramePercentAveReset##Metrics	0				
unFrameThroughputPercent[]##Metrics	56	51	32	51	67
unInterruptTimes[]##Metrics	289	484	471	298	363
unMaxFrameInterruptTime##Metrics	1100				
unMaxNestedInterruptTime##Metrics	505				

Figure-6 Desired Throughput outcome

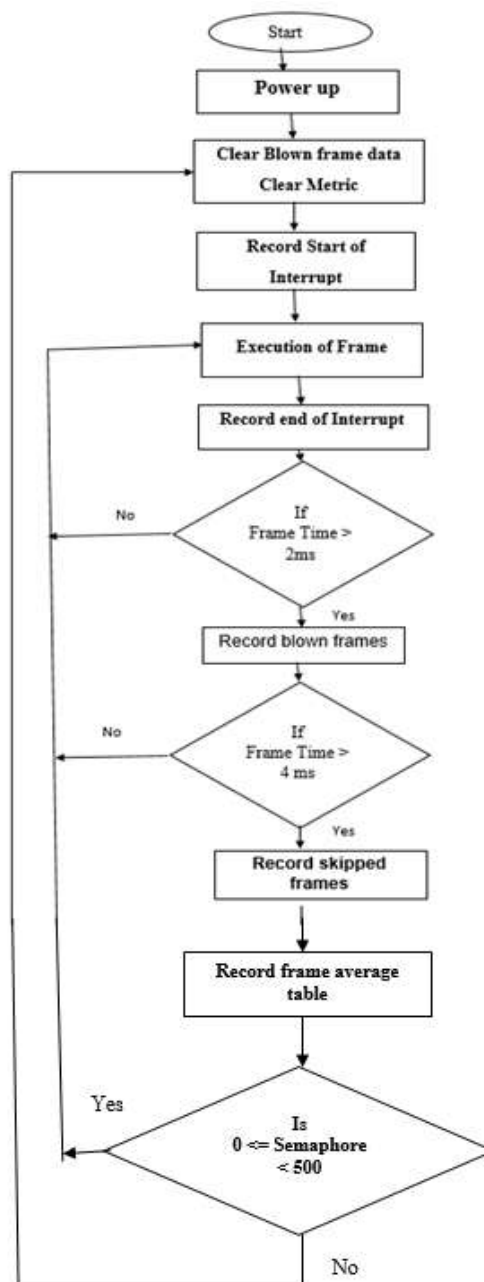

Figure-5 Technical flow process of monitoring tool of time frame.

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Analysing the root cause of these fault code and troubleshooting should be done for proper functioning of Genset and initialization of the test. Ultimately, checking the Utility of Modbus register and obtaining the throughput values. If the throughput value obtained is more than the desired throughput range, then software scripts should be modified. These updated scripts should be calibrated on the Gensets boards and the throughput testing should be processed again.
Here, figure-6 shows the test report sheet obtained from the Monitoring tool after simulation. The throughput value obtained in this test is 56%.

V. CONCLUSION

This paper depicts about the development of Throughput testbench setup, its implementation and Simulation. The aim for development of this testbench is to achieve the Throughput value in the desired range of 50-60% for Memory Expanded Genset board is achieved by making the 'umskippedFrame' value to zero. Thus the desired Throughput value suffices the markets needs i.e. advanced features required by the users for the better performance of the gensets. Moreover, on achieving the desired throughput range, the board will be capable of adding extensive advance features.

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